REMARKS

In the Office Action, claims 1-6 are rejected under the judicially created doctrine of obviousness-type double patenting in view of U.S. Patent 6,829,756. In response to the rejection, Applicant submits a terminal disclaimer in compliance with 37 CFR 1.321(c) to overcome the rejection. Claims 1-6 are also rejected under 35 USC §102(b) as being anticipated by Selvidge et al. (U.S. Patent 5,850,53 "Selvidge").

In response to the rejection of claims 1-6 under 35 USC §102(b) as being anticipated by Selvidge, Applicant respectfully submits that claims 1 and 2 clearly distinguish over Selvidge. Independent claim 1 recites steps of:

> "merging a set of nets carrying signals into a shared interconnect portion; and
> altering a netlist based on the merging."

Similarly, independent claim 2 is directed to a method of multiplexing signals in a programmable logic device, and includes steps:

> "merging nets into a shared interconnect portion, and
> altering the design based upon the merging."

Selvidge relates to a system for emulating a logic design. However, Selvidge teaches away from Applicant's claims by dividing a netlist into logic partition blocks to be loaded into multiple FPGAs of the emulation system. As shown in Fig. 1B, the netlist 20 is separated into logic partition blocks 22, each of which is implemented in a single FPGA chip 12 of the network 8. The logic signal connections 24 that bridge the partition blocks are provided by the interconnect 14. (Col. 5, lines 13-19). In contrast to Selvidge which divides a netlist, Applicant claim in claim1 merging a set of nets and altering a netlist based on the merging. In further contrast to Selvidge which multiplexes signals between FPGAs, Applicant also claims in claim 2 merging nets and altering a design to multiplex signals in a programmable logic device. Accordingly, Applicant respectfully requests reconsideration of the rejection of claims 1 and 2.

In response to the rejection of claims 3-6, Applicant has amended independent claim 3 in order to overcome the rejection. In particular, Applicant has amended

independent claim 3 to indicate that the set of configurable logic blocks of the programmable logic device comprises "multiple signal sources and at least one destination." Applicant has also amended claim 3 to recite "a programmable interconnect point coupled between the output of the time multiplexing signal generator and the destination configurable logic block." Applicant respectfully submits that claim 3 as amended distinguishes over Selvidge. Selvidge comprises a network 8 having an array of individual FGPA chips 12. Applicant's claim 3 as amended is directed to an integrated circuit having both source and destination configurable logic blocks, and a programmable interconnect coupled to a destination configurable logic block of the integrated circuit. Applicant respectfully requests reconsideration of claim 3 as amended and dependent claims 4-6.

Applicant has added new dependent claims 7-20 which are based upon independent claims 1-3. Applicant submits that the new claims are also allowable over Selvidge for the same reason that the independent claims are believed allowable, and that no new matter is added by the claims.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on May 2, 2005.

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